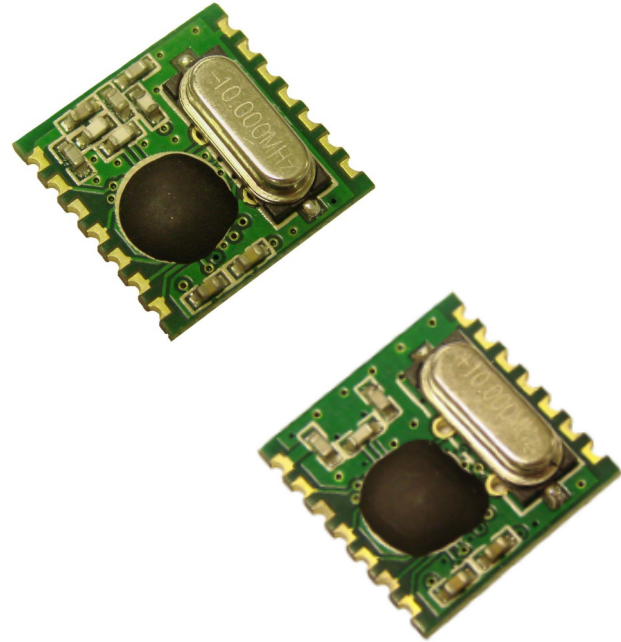


ALPHA RF Modules

Features

- FM Transmitter & Receiver Modules
- Available as 433 or 915MHz
- Transmit Range up to 300m
- Miniature SMT Packages
- Data Rate up to 256Kbps
- Programmable Output Power
- 2.2 – 5.4Vdc Operating Voltage
- Standby Current <300nA
- Programmable Freq Deviation
- SPI Interface (for Config)
- Clock and Reset Signal for External MCU
- Wakeup Timer
- Automatic Antenna Tuning
- Differential Antenna Output
- Low Battery Detection
- EMC Compliant , FCC Compliant
- Operates from -45 to +85°C



Transmitter

- 2.2-5.4v Supply Voltage
- Programmable Output Power

Receiver

- Standby current < 0.3uA
- Wake up timer function
- PLL Design
- Digital Signal Strength indicator
- Programmable receive bandwidth (67 to 400KHz)

Applications

- Wireless Security Systems
- Car Alarms
- Remote Gate Controls
- Remote Sensing
- Data Capture
- Sensor Reporting

Introduction

The Alpha Modules are extremely cost effective but high performance radio modules. Supplied in a miniature Surface mount package these modules can Transmit/Receive at upto 115Kbps at upto 300m range.

Operating at 2.2-5V, both transmitter and receiver monitor their battery voltage and can sleep with very low standby current. The modules can wake intermittently and provide direct control outputs to a microcontroller, ideally suited to battery applications. (Especially receivers!)

These Modules will suit one to one multi-node wireless links in applications including car and building security, POS and inventory tracking, remote process monitoring.

ALPHA RF Modules

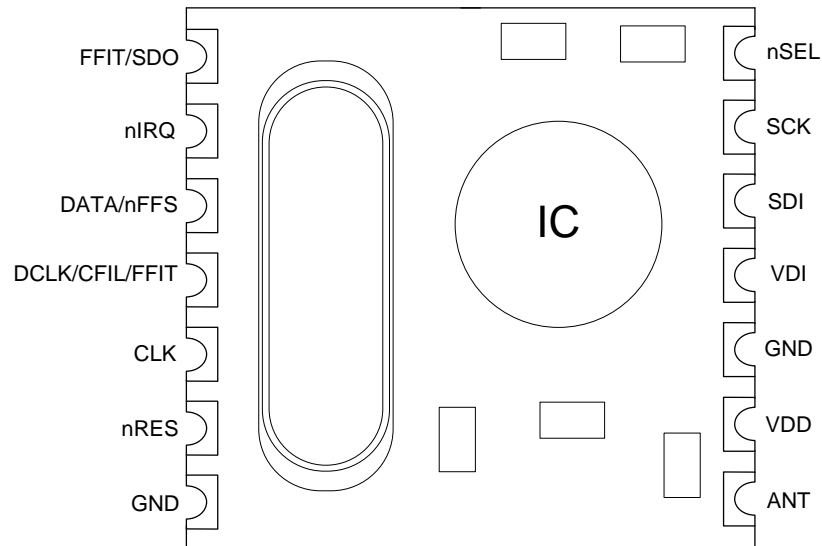


Part Number	Description
ALPHA-TX433S	FM Transmitter Module 433MHz
ALPHA-	
ALPHA-	
ALPHA-	
ALPHA-	
ALPHA-	

Transmitter Pin Description

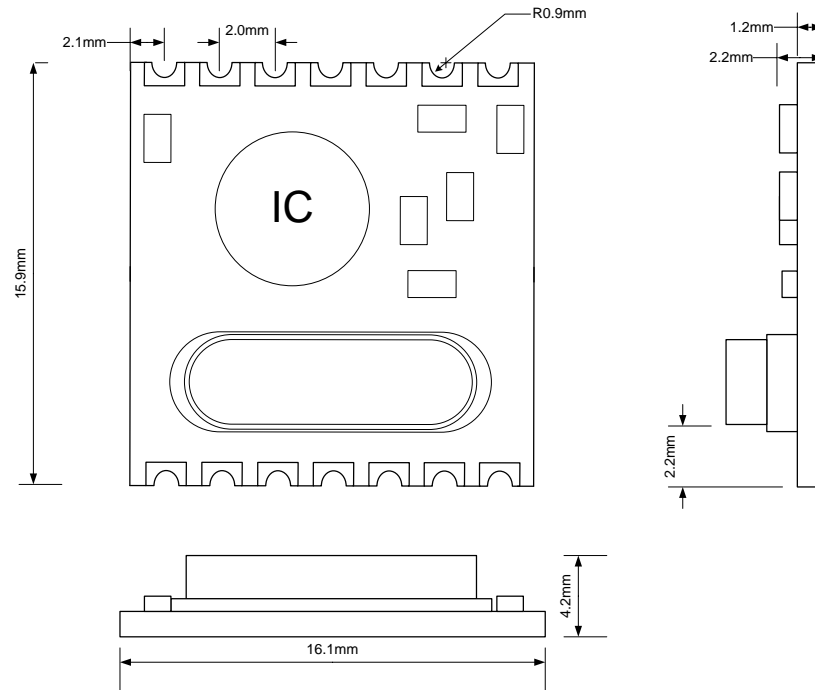
			Interrupt Request Out (Active Low)

Receiver Pin Description

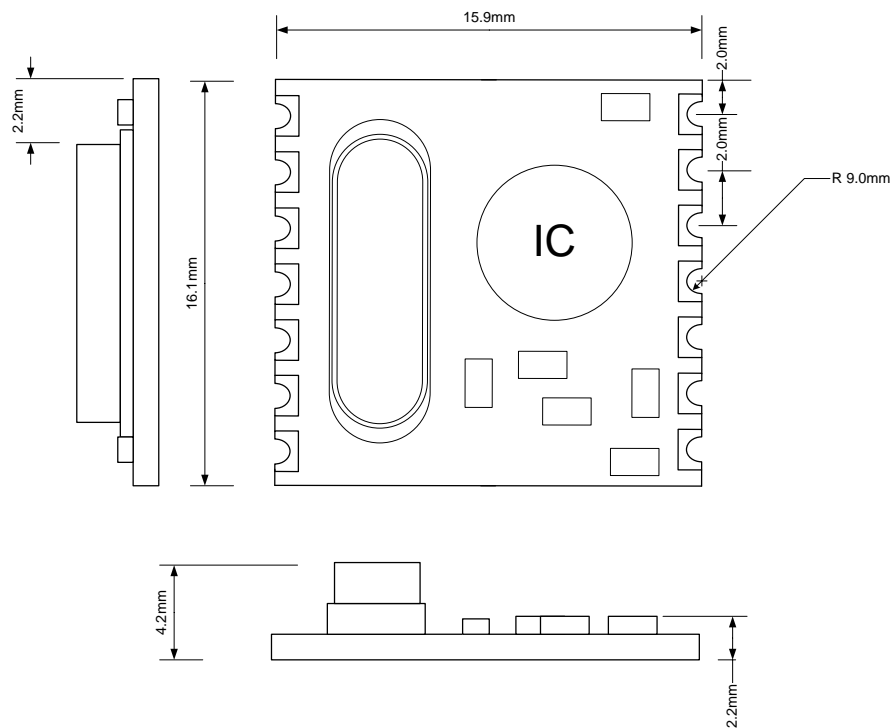


	FFIT/SDO		FIFO fill interrupt (Active Low) / status read data output
	nIRQ		Interrupt Request Output (Active Low)
	DATA/nFFS		FSK Data Output (non FIFO Mode) / FIFO Select
	DATA/CFIL/FFIT	IN/OUT	Clock Output (noFIFO) / External filter Capacitor(analog mode) / FIFO interrupt (active High) when FIFO level set to 1, FIFO Empty interruption can be achieved.
5			
6	nRES		Reset Device
7			
			Antenna input
9			
10			
	VDI		Valid Data Indicator
	nSEL		

Transmitter Mechanical Dimensions



Receiver Mechanical Dimensions



ALPHA RF Modules



Receiver Technical Specifications

Maximum Ratings (not Operating)

Symbol	Parameter	Minimum	Maximum	Unit
V _{DD}	Positive Supply	-0.5	6.0	V
V _{IN}	All pin input level	-0.5	V _{DD} +0.5	V
I _{IN}	Input current except power	-25	+25	mA
T _{ST}	Storage Temp	-55	125	°C
T _{ID}	Soldering Temp		260	°C

Maximum Working Range

Symbol	Parameter	Minimum	Maximum	Unit
V _{DD}	Positive Supply	2.2	5.4	V
T _{OP}	Operating Temp	-40	85	°C

DC Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
I _{DD}	Current Consumption @ 433 @ 915		9	11	mA
			10.5	12.5	
I _X	Stand by Current		3.0	3.5	mA
I _{PD}	Sleep Mode Current		0.3		uA
I _{LB}	Low Battery Detection		0.5		uA
V _{LB}	Low Battery Step (0.1V steps)	2.2		5.3	V
V _{LBA}	Low Battery accuracy		75		mV
V _{IL}	Low Level Input			0.3 x V _{DD}	V
V _{IH}	High Level Input	0.7 x V _{DD}			V
I _{IL}	Leakage Current, V _{IL} = 0V	-1		1	uA
I _{IH}	Leakage Current, V _{IH} = V _{DD} , V _{DD} = 5.4V	-1		1	uA
V _{OL}	Low Level output, I _{OL} = 2mA			0.4	V
V _{OH}	High Level output, I _{OH} = 2mA	V _{DD} -0.4			V

AC Characteristics

Symbol	Parameter	Min	Typical	Max	Unit
F _{LO}	Frequency @433MHz @915MHz	430.24		439.75	MHz
		900.72		929.27	
BW	Bandwidth	1	60	75	KHz
		2	120	150	
		3	180	225	
		4	240	300	
		5	300	375	
		6	360	450	
T _{LOCK}	PLL Lock time, after 10MHz step hopping.		20		uS
T _{ST,P}	PLL Start time, after crystal stabilised		250		uS
BR	Data Rate			115.2	Kbps
P _{MIN}	Sensitivity @433MHz @915MHz		-109	-100	dBm
			-105	-98	
RS _A	RSSI Accuracy	-5		+5	dB
RS _R	RSSI Range		46		dB
RS _{STEP}	RSSI Programmable Step		6		dB
RS _{ARSSI}	ARSSI Filter		1		nF
RS _{RESP}	DRSSI Response Time, C		500		us
C _{XL}	Capacitor Bank	8.5		16	pF
T _{POR}	PWR time, power up time (V _{DD} to 90%)		50	100	mS
T _{PBT}	Wake up timer period	.96		1.08	mS
T _{WAKEUP}	Programmable Wake up time	1		5x10 ¹¹	mS

Transmitter Technical Specifications

Maximum Ratings (not Operating)

Symbol	Parameter	Minimum	Maximum	Unit
V _{DD}	Positive Supply	-0.5	6.0	V
V _{IN}	All pin input level	-0.5	V _{DD} +0.5	V
I _{IN}	Input current except power	-25	+25	mA
T _{ST}	Storage Temp	-55	125	°C
T _{ID}	Soldering Temp		260	°C

Maximum Working Range

Symbol	Parameter	Minimum	Maximum	Unit
V _{DD}	Positive Supply	2.2	5.4	V
T _{OP}	Operating Temp	-40	85	°C

DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
I _{DD}	Current Consumption @ 433MHz @ 915MHz @ 0dBm Power output		12 15		mA
I _{DD}	Current Consumption @ max power output		23		mA
I _{PD}	Sleep Mode Current		0.3		uA
I _{WT}	Wake up timer consumption		1.5		uA
I _{LB}	Low Battery Detector Current		0.5		uA
I _X	Idle Mode (crystal only)		1.5		mA
V _{LB}	Low Battery Detect range (0.1V steps)	2.2		5.3	mV
V _{IL}	Low Level Input			0.3 x V _{DD}	V
V _{IH}	High Level Input	0.7xV _{DD}			V
I _{IL}	Leakage Current, V _{IL} = 0V	-1		1	uA
I _{IH}	Leakage Current, V _{IH} = V _{DD} , V _{DD} = 5.4V	-1		1	uA
V _{OL}	Low Level output, I _{OL} = 2mA			0.4	V
V _{OH}	High Level output, I _{OH} = 2mA	V _{DD} -0.4			V

AC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F _{REF}					
F ₀	Frequency @433MHz 2.5KHz Step @915MHz 7.5KHz Step	430.24 900.72		439.75 929.27	MHz
T _{LOCK}	PLL Lock time, after 10Mhz step hopping.		20		uS
T _{SP}	PLL Start time, after crystal stabilised			250	uS
P _{MAX}	Max Available Power Output @433MHz @915MHz	5 2	7 4		dBm
Q ₀	Q Factor of Output capacitance	16	18	22	
BR _{FSK}	FSK Data Rate			115.2	kbps
DF _{FSK}	FSK Deviation, 30KHz step	30		210	KHz
T _{PBT}	Period for Wake Up timer	0.95		1.05	mS
T _{WAKEUP}	Wake Up Timer	1		2x10 ⁹	mS
T _{PQR}	Power up time		100		mS

Transmitter Programming Guide

1. Brief Description

The ALPHA Transmitter is a low cost FSK transmitter. It needs only an MCU, crystal, decoupling capacitor and antenna to build a high reliability FSK transmitter. The operation frequency can cover 300 to 1000MHz. The module supports a command interface to setup frequency, deviation, output power and also data rate.

Control Command	Related Parameters/Functions		Related control bits
1	Configuration Setting Command	Frequency band, microcontroller clock output, crystal load capacitance, frequency deviation	b1 to b0, d2 to d0, x3 to x0, ms, m2 to m0
2	Power Management Command	Crystal oscillator, synthesizer, power amplifier, low battery detector, wake-up timer, clock output buffer	a1 a0, ex, es, ea, eb, et, dc
3	Frequency Setting Command	Carrier frequency	f11 to f0
4	Data Rate Command	Bit rate	r7 to r0
5	Power Setting Command	Nominal output power, OOK mode	ook, p2 to p0
6	Low Battery Detector Command	Low battery threshold limit, transmit bit synchronizer, wake-up timer calibration	dwc, ebs, t4 to t0
7	Sleep Command	Length of the clock tail after power down	s7 to s0
8	Push-Button Command	Push-button related functions	p4, d1 to d0, b4 to b1, bc
9	Wake-Up Timer Command	Wake-up time period	r4 to r0, m7 to m0
10	Data Transmit Command		Data transmission
11	Status Register Command		Transmitter status read
12	PLL Setting and Reset Mode Command	PLL bandwidth, reset mode	bw1 to bw0, dr

2. Commands

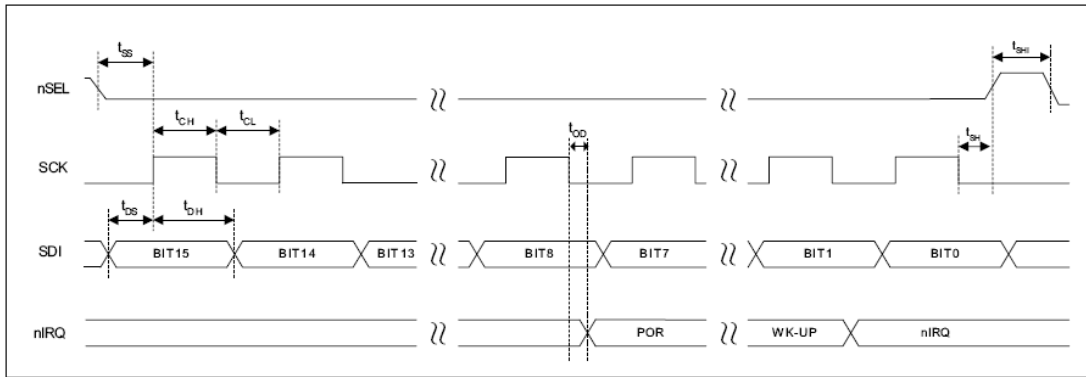
CONTROL INTERFACE

Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10
t_{BL}	Push-button input low time	25

1. Timing Diagram



2. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	d2	d1	d0	x3	x2	x1	x0	ms	m2	m1	m0	8080h

b1..b0: band select:

b1	b0	band[MHz]
0	1	433
1	0	868
1	1	915

d2..d0: select frequency of CLK pin

d2	d1	d0	CLK frequency[MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derived from the crystal oscillator and can be applied to the MCU clock in to save a second crystal. If not used, please set bit "dc" to disable CLK output

x3..x0: select crystal load capacitor

x3	x2	x1	x0	Load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
.....			
1	1	1	0	15.5
1	1	1	1	16.0

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software.

ms: select modulation polarity
m2..m0: select frequency deviation

m2	m1	m0	Frequency deviation[kHz]
0	0	0	30
0	0	1	60
0	1	0	90
0	1	1	120
1	0	0	150
1	0	1	180
1	1	0	210

3. Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	a1	a0	ex	es	ea	eb	et	dc	C000h

a1: Crystal oscillator and synthesizer are enabled by Data transmit Command and disable by Sleep command.

a0: Power amplifier is enabled by Data transmit Command and disable by Sleep Command.

ex: Enable crystal oscillator

es: Enable synthesizer

ea: Enable power amplifier

eb: Enable low battery detection function

et: Enable wake-up timer

4. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A7D0h

The 12-bit parameter of the Frequency Setting Command <f11- f0> has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f0 can be calculated as:

$$f_0 = 10 \text{ MHz} * C_1 * (C_2 + F/4000)$$

The constants C1 and C2 are determined by the selected band as:

Band	C1	C2
315	1	31
433	1	43
868	2	43

5. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	r7	r6	r5	r4	r3	r2	r1	r0	C800h

r7..r0: set data rate
 $BR=10000000/29/(R+1)$
 BR is data rate

Apart from setting custom values, the standard bit rates from 2.4 to 115.2 kbps can be approximated with minimal error.

The commands are read out with a different fixed bit rate:

Fsck = 10 MHz / 29 / 3 [~115.2 kHz]

Note:

PLL bandwidth should be set according the data rate. Please see the PLL Setting Command

6. Power Setting Command

bit	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	p2	p1	p0	B0h

p2..p0: set relative output power:
 $P_{out}=P_{max}-P*3$ [dBm]
 Pmax is the max output power; it is related to the antenna impedance.

7. Low Battery Detector and Tx bit Synchronization Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	dwc	0	ebs	t4	t3	t2	t1	t0	C200h

dwc: Disable wake-up timer periodical calibration
 ebs: Enable TX bit synchronization function
 t4..t0: Set threshold voltage of Low battery detector
 $V_{lb}=2.2+T*0.1$ [V]

8. Sleep Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0	C400h

If crystal oscillator, synthesizer and power amplifier are auto-controlled, this command will close power amplifier and synthesizer immediately, then stop crystal oscillator after S periods of CLK signal

9. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E00h

The wake-up timer period is determined by:
 $T_{wake-up} = M * 2R$ [ms]
 For continual operation, bit 'et' must be cleared and set

10. Data Transmit Command

bit	7	6	5	4	3	2	1	0
	1	1	0	0	0	1	1	0

This command indicate that the following data on SDI pin is to be transmitted, the transmission stops if nSel return to hi.

11. Status Register Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	--

With this command, it is possible to read the chip's status register through the nIRQ pin. This command clears the last serviced interrupt and processing the next pending one will start (if there is any).

12. PLL Setting and Reset Mode Command

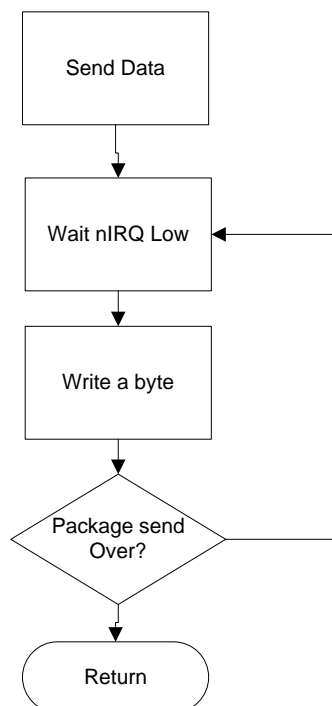
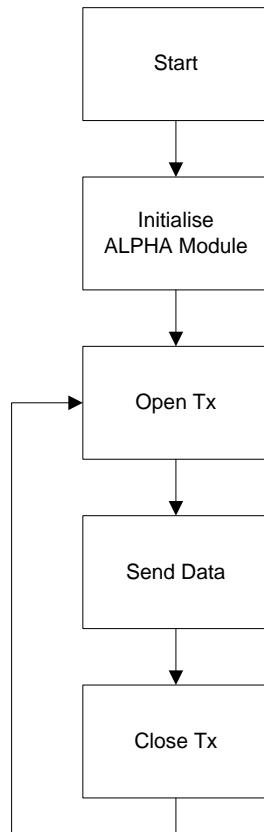
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
1	1	0	1	0	0	1	0	bw1	bw0	0	0	0	0	dr	0	D200h

Bits 7-6 <bw1 : bw0> select the PLL bandwidth:

Bw1	bw0	Max datarate [kbps]
0	1	19.2
1	1	38.4
0	0	68.9
1	0	115.2

Bit 1 (dr): Disables the highly sensitive RESET mode. If this bit is cleared, a 600 mV glitch in the power supply may cause a system reset. For more detailed description see the Reset modes section.

3. Transmitter Operation Flow



Receiver Programming Guide

4. Brief Description

The ALPHA Receiver is a low cost FSK Receiver with all RF functions integrated. It needs only an MCU, crystal, decoupling capacitor and antenna to build a high reliability FSK transmitter. The operation frequency can cover 300 to 1000MHz. Although each module can cover all frequencies, better performance is obtained by using the module at the pre-set frequency

The module supports a command interface to setup frequency, deviation, output power and also data rate.

5. Commands

CONTROL INTERFACE

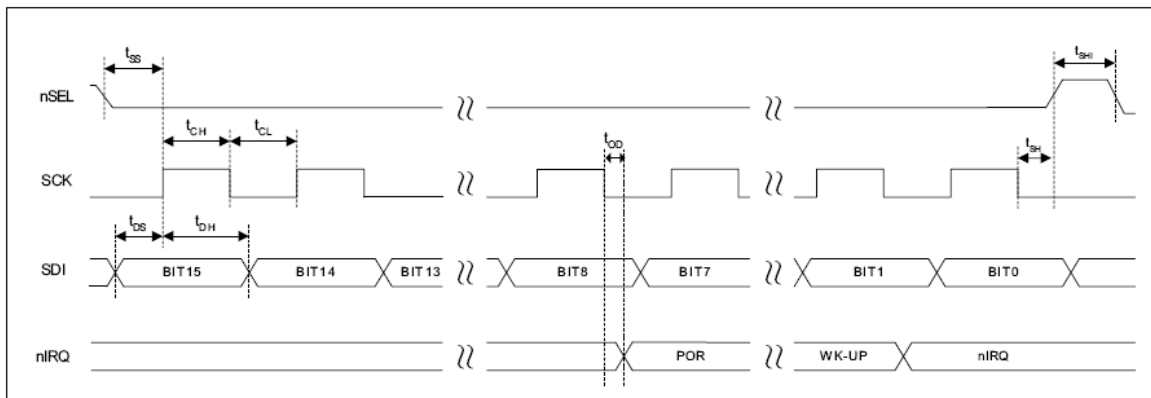
Commands to the transmitters are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

The status information or received data can be read serially over the IRQ pin. Bits are shifted out upon the falling edge of CLK signal (POR) circuit sets default values in all control and command registers.

The status information or received data can be read serially over the IRQ pin. Bits are shifted out upon the falling edge of CLK signal

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10
t_{BL}	Push-button input low time	25



1. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	893Ah

b1..b0: band select:

b1	b0	band[MHz]
0	0	315
0	1	433
1	0	868
1	1	915

eb: Enable low battery detection function

et: Enable wake-up timer

ex: Enable crystal oscillator

x3..x0: select crystal load capacitor

x3	x2	x1	x0	load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
.....
1	1	1	0	15.5
1	1	1	1	16.0

i2..i0:select baseband bandwidth

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

dc: Disable signal output of CLK pin

2. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

f11..f0: Set operation frequency

The 12-bit parameter of the *Frequency Setting Command* <f11- f0> has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f0 can be calculated as:

$$f0 = 10 \text{ MHz} * C1 * (C2 + F/4000)$$

The constants C1 and C2 are determined by the selected band as:

Band	C1	C2
315	1	31
433	1	43
868	2	43

3. Receiver Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C0C1h

d1..d0: select VDI source

d1	d0	VDI output
0	0	Digital RSSI output(DRSSI)
0	1	Data quality detection output (DQD)
1	0	Clock recovery lock output
1	1	DRSSI & DQD

g1..g0: select LNA gain

g1	g0	LNA gain (dBm)
0	0	0
0	1	-14
1	0	-6
1	1	-20

r2..r0: select DRSSI threshold

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	-67
1	0	1	-61

The actual DRSSI threshold is related to LNA setup:
 $RSSI_{th} = RSSI_{setth} + G_{LNA}$
 en: Enable the receiver

4. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up period is determined by:

$$T_{wake-up} = M * 2^R [ms]$$

For continual operation, bit 'et' must be cleared and set

5. Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	en	CCOEh

d6..d0: Set duty cycle D.C. = $(D * 2 + 1) / M * 100\%$

en: Enable low duty cycle mode

6. Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	t4	t3	t2	t1	t0	C200h

d2..d0: select frequency of CLK pin

d2	d1	d0	Clock frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal. If not used, please set bit "dc" to disable CLK output

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

t4..t0: Set threshold voltage of Low battery detector: $V_{lb} = 2.2 + T * 0.1 [V]$

7. AFC Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	r1	r0	st	fi	oe	en	C6F7h

a1..a0: select AFC auto-mode:

a1	a0	
0	0	Controlled by MCU
0	1	Run once at power on
1	0	Keep offset when VDI hi
1	1	Keeps independently from VDI

r1..r0: select range limit

r1	r0	range (fres)
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3-4

Freq

315 & 433band: 2.5kHz

868band: 5kHz

915band: 7.5kHz

st: st goes hi will store offset into output register

fi: Enable AFC hi accuracy mode

oe: Enable AFC output register

en: Enable AFC function

8. Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	al	ml	1	s1	s0	f2	f1	f0	C42Ch

al: Enable clock recovery auto-lock

ml: Enable clock recovery fast mode

s1..s0: select data filter type

s1	s0	Filter type
0	0	OOK
0	1	Digital filter
1	0	reserved

f1..f0: Set DQD threshold

9.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C823h

The expected bit rate of the received data stream is determined by the 7-bit value R (bits r6 to r0) and the 1 bit cs.

$$BR = 10000000 / 29 / (R + 1) / (1 + cs * 7)$$

In the receiver set R according the next function:

$$R = (10 \text{ MHz} / 29 / (1 + cs * 7) / BR) - 1$$

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

10. Outputs and FIFO mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE85h

f3..f0: Set FIFO interrupt level

s1..s0: select FIFO fill start condition

s1	s0	
0	0	VDI
0	1	Sync-word
1	0	VDI & Sync-word
1	1	Always

ff: Enable FIFO fill

fe: Enable FIFO function

11. Reset Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	dr	DA00h

Bit 0 (*dr*): Disables the highly sensitive RESET mode. If this bit is cleared, a 600 mV glitch in the power supply may cause a system reset. For a more detailed description see the *Reset modes* section.

12. Status Read Command

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the module identifies it as a read command. So as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:-

FIFO IT	Number of the data bits in the FIFO is reached the preprogrammed limit
FFOV	FIFO overflow
WK-UP	Wake-up timer overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
FFEM	FIFO is empty
DRSSI	The strength of the incoming signal is above the preprogrammed limit
DQD	Data Quality Detector detected a good quality signal
CRL	Clock recovery lock
ATGL	Toggling in each AFC cycle
ASAME	AFC stabilized (measured twice the same offset value)
OFFS6, 4-0	Offset value to be added to the value of the Frequency control word

Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (*FIFO IT - LBD*) to clear the FFOV, WK-UP, and LBD bits. During the FIFO access the fSCK cannot be higher than $f_{ref} / 4$, where f_{ref} is the crystal oscillator frequency. If the FIFO is read in this mode the nFFS input must be connected to logic high level.

FIFO Buffered Data Read

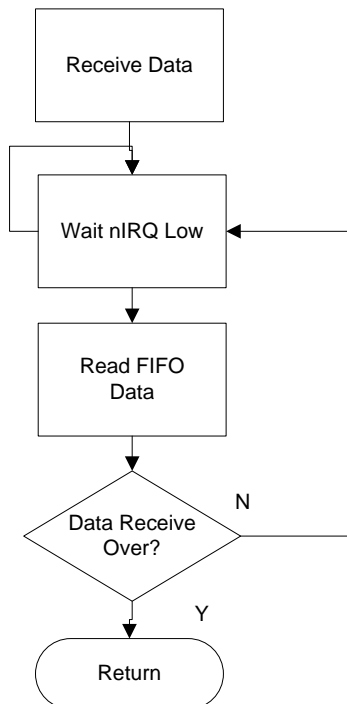
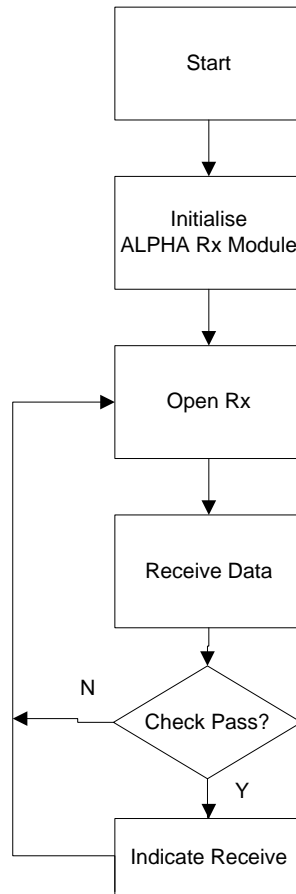
In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

For further details see the *Receiver Setting Command* and the *Output and FIFO Command*.

Polling Mode: The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:

The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.



After Initialisation, open FIFO receive mode and wait for nIRQ low, only then can the MCU read received and stored data in FIFO.
For the next received package please reset FIFO

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